REMARKS

The Office Action dated July 17, 2009 was received and carefully reviewed.

Claims 1-13 were pending in the subject application prior to this response. Presently, claims 1-4 are amended to clarify the invention, and not for reasons of patentability. Claims 10-13 remain withdrawn for being directed to a non-elected invention. No new claims have been added, and no claims have been canceled. Accordingly, claims 1-13 remain pending in the subject application.

Support for the amendments to claims 1-4 can be seen on page 12, lines 17-25, as well as page 16, lines 7-19, and FIG. 4 of the specification as originally filed. Accordingly, Applicants contend that the amendment to the claims do not include new matter.

Reconsideration and withdrawal of the currently pending rejections are hereby requested in view of the following remarks.

Claim Rejections - Prior Art

Claims 1-4, 7, and 9 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Yamazaki (U.S. Patent No. 6,891,236 B1). Claims 1-9 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Fujii et al. (U.S. Pat. Pub. No. 2005/0074963 A1) in view of Yu (U.S. Patent No. 6,323,143 B1). Applicants traverse the rejections for at least the reasons set forth below.

Applicants respectfully submit that independent claims 1-4, and the claims dependent therefrom, are patently distinguishable over *Yamazaki*, *Fujii*, and *Yu*, since *Yamazaki*, *Fujii*, and *Yu* fail to disclose, teach, or suggest all of the features recited in the pending claims. For example, independent claim 1 (emphasis added) recites:

> 1. A light-emitting device comprising:
> a light-emitting element in which a light-emitting material is sandwiched between a pair of electrodes in a pixel; and
> a thin film transistor including, from a substrate side, a lamination of:
> **a base layer;**

a gate electrode formed by fusing conductive nanoparticles over the base layer;

a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide; and

a semiconductor layer,

wherein the base layer is formed from a metal material and the base layer not overlapping with the gate electrode is oxidized, and

wherein the light-emitting element and the thin film transistor are connected in the pixel.

Independent claim 2 (emphasis added) recites:

2. A light-emitting device comprising:

a light-emitting element in which a light-emitting material is sandwiched between a pair of electrodes in a pixel; and

a thin film transistor including, from a substrate side, a lamination of:

a base layer;

a gate electrode formed by fusing conductive nanoparticles over the base layer;

a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide;

a semiconductor layer;

wirings connected to a source and a drain and formed by fusing conductive nanoparticles; and

a silicon nitride layer or silicon nitride oxide layer formed by being in contact with the wirings,

wherein the base layer is formed from a metal material and the base layer not overlapping with the gate electrode is oxidized, and

wherein the light-emitting element and the thin film transistor are connected in the pixel.

Independent claim 3 (emphasis added) recites:

3. A light-emitting device comprising:

a light-emitting element in which a light-emitting material is sandwiched between a pair of electrodes in a pixel;

a first thin film transistor including, from a substrate side, a lamination of:

a base layer;

a gate electrode formed by fusing conductive nanoparticles over the base layer;

a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide; and

a semiconductor layer;

a driver circuit including a second thin film transistor formed by having the same layer structure as that of the first thin film transistor; and

a wiring extended from the driver circuit and connecting to the gate electrode of the first thin film transistor,

wherein the base layer is formed from a metal material and the base layer not overlapping with the gate electrode is oxidized, and

wherein the light-emitting element and the thin film transistor are connected in the pixel.

Independent claim 4 (emphasis added) recites:

4. A light-emitting device comprising:

a light-emitting element in which a light-emitting material is sandwiched between a pair of electrodes in a pixel;

a first thin film transistor including, from a substrate side, a lamination of:

a base layer;

a gate electrode formed by fusing conductive nanoparticles over the base layer;

a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide;

a semiconductor layer;

wirings connected to a source and a drain and formed by fusing conductive nanoparticles; and

a silicon nitride layer or silicon nitride oxide layer formed to be in contact with the wirings;

a driver circuit including a second thin film transistor formed by having the same layer structure as that of the first thin film transistor; and

a wiring extended from the driver circuit and connecting to the gate electrode of the first thin film transistor,

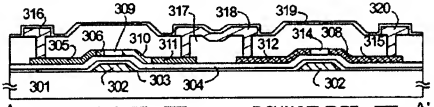
wherein the base layer is formed from a metal material and the base layer not overlapping with the gate electrode is oxidized, and

wherein the light-emitting element and the thin film transistor are connected in the pixel.

As seen above, independent claims 1-4 are directed to, *inter alia*, the features of a base layer, a gate electrode formed by fusing conductive nanoparticles over the base layer, wherein the base layer is formed from a metal material and the base layer not overlapping with the gate electrode is oxidized.

Applicants contend that *Yamazaki*, *Fujii*, and *Yu*, taken either alone or in combination, fail to anticipate or render obvious at least the features of a base layer, a gate electrode formed by fusing conductive nanoparticles over the base layer, wherein the base layer is formed from a metal material and the base layer not overlapping with the gate electrode is oxidized, as recited in present independent claims 1-4.

Yamazaki appears to disclose a semiconductor device including a substrate 301, a gate electrode 302 formed directly on the substrate 301, a first insulating film 303, a second insulating film 304, source region 305, drain region 311, channel region 309, and active regions 306 and 310 (see *Yamazaki*, e.g., FIG. 7B and col. 14, ll. 4-42). As seen in the figure below, it appears that no base layer is formed between the gate electrode 302 and the substrate in *Yamazaki*.



SECTIONAL STRUCTURE VIEW ALONG A-A'

FIG. 7B

Thus, Applicants contend that *Yamazaki* appears to remain completely silent with regard to "a base layer, a gate electrode formed by fusing conductive nanoparticles over the base layer, wherein the base layer is formed from a metal material and the base layer not overlapping with the gate electrode is oxidized", as recited in present independent claims 1-4.

On page 9 of the Office Action, the Examiner alleges that *Fujii* discloses "a gate insulating layer (106) formed in contact with the gate electrode (106) [*sic*], at least containing a

layer comprising a silicon nitride (par. 52)". However, as seen below in FIG. 1A of *Fujii*, the gate electrode 104 appears to be formed directly on the substrate 100, and not formed over a base layer at all, let alone a base layer formed from a metal material and wherein the base layer not overlapping with the gate electrode is oxidized, as in present independent claims 1-4.

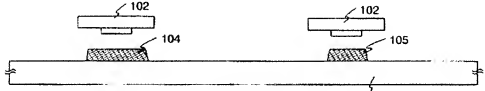


FIG. 1A

For at least the reasons stated above, it appears that *Fujii* fails to disclose, teach, or suggest the features of a base layer, a gate electrode formed by fusing conductive nanoparticles over the base layer, wherein the base layer is formed from a metal material and the base layer not overlapping with the gate electrode is oxidized, as recited in present independent claims 1-4.

Applicants contend that *Yu* fails to remedy the above-recited deficiencies with respect to *Fujii*. Therefore, since neither *Yamazaki*, *Fujii*, nor *Yu*, taken either alone or in combination, anticipate or render obvious each and every feature recited in present independent claims 1-4, the Examiner has failed to provide a proper *prima facie* case of obviousness with respect to independent claims. Consequently, Applicants respectfully request the withdrawal of the rejection under 35 U.S.C. § 102(e) and 103(a), and the allowance of independent claims 1-4.

Claims 5-9 are also allowable at least by virtue of their dependency from one of the independent claims, but also because they are distinguishable over the prior art. Thus, it is respectfully requested that the rejection be withdrawn, and that claims 5-9 receive allowance.

In view of the foregoing, it is submitted that the present application is in condition for allowance and a notice to that effect is respectfully requested. If, however, the Examiner deems that any issue remains after considering this response, the Examiner is invited to contact the undersigned attorney/agent to expedite the prosecution and engage in a joint effort to work out a mutually satisfactory solution.

Except for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 19-2380. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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